AMENDMENTS TO CLAIMS

Please amend claims as follows.

Claims 1-9 (canceled).

10. (currently amended) A structure of a flash memory, comprising:

a substrate ;

a floating gate disposed on the substrate, wherein the floating gate comprises:

a patterned conductive layer disposed on the substrate; and

a conductive spacer disposed on first both sidewalls of the patterned conductive layer, wherein a top surface of the conductive spacer and a top surface of the patterned conductive layer are located at a same level;

a tunnel oxide layer disposed between the substrate and the floating gate;

a control gate disposed on the floating gate;

an inter-poly dielectric disposed between the control gate and the floating gate, wherein a stacked gate structure is constructed by the tunnel oxide layer, the floating gate, the inter-poly dielectric and the control gate; and

a source region and a drain region, disposed in both side of the stacked gate structure within the substrate.

11. (original) The structure of a flash memory of claim 10, wherein a material of the conductive layer comprises a doped polysilicon.

12. (original) The structure of a flash memory of claim 10, wherein a material of the conductive spacer comprises a doped polysilicon.

13. (currently amended) The structure of a flash memory of claim 10, wherein the source region and the drain region are disposed in the substrate adjacent second both sidewalls of the conductive layer without the conductive spacer.